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Patent Application Transmittal

Transmitted herewith for filing is the Patent Application of:

Inventors(s): Brian Keith Bullis, John Charles Goss, Robert Brian Likovich, Jr.

For: ASYNCHRONOUS DATA BUFFER AND A METHOD OF USE THEREOF

Enclosed are

14 pages of specification, including *22* claims, plus *4* sheets of drawings.

x An assignment of the invention to International Business Machines Corporation, Armonk, New York 10504.

A certified copy of a/an application.

x Declaration and Power of Attorney.

x PTO-1449 & references

x A return post card

Other:

Filing Fee Calculation (For Other Than Small Entity)

Basic Fee:						$690.00
Claims Fees:	Filed	Limit	Extra		Rate per Extra	
Total claims:	22	20	2		$18.00	$36.00
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ASYNCHRONOUS DATA BUFFER AND A METHOD OF USE THEREOF

FIELD OF THE INVENTION

The present invention relates generally to network data transfer systems and specifically to an asynchronous data buffer and a method of use thereof.

BACKGROUND OF THE INVENTION

Many conventional network data transfer systems utilize cell relay systems to transfer data. The objective of cell relay systems is to develop a single high-speed network based on a switching and multiplexing scheme that works for all data types. Cell relay is a generic term for a packet switching protocol using fixed length packets or cells. A packet or cell is a bundle of data, usually in binary form, organized in a specific way for transmission.

A network data transfer system ordinarily involves a sending device and a receiving device. However, because the sending device usually has a different data rate/flow than the receiving device, data buffers typically are utilized. A buffer is a temporary storage location for information being sent or received and is located between two different devices that have different rates for handling the data. Figure 1 is an example of a typical data transfer environment. This environment includes a sending device 10, a buffer 12, and a receiving device 14. The buffer 12 includes a write element 11 for writing data cells into the buffer 12 from the sending device 10 and a read element 13 for reading data cells from the buffer 12 to the receiving device 14. Basically, the buffer acts like a dam. It captures the data cells from the sending device 10 and then sends them out at a rate that can be handled by the receiving device 14.

However, conventional systems require that each data cell being transferred be

completely written into the buffer 12 before it can be read out. A problem with this type of implementation is the latency involved during data transfer. Latency is the time elapsed from when the data cell first enters the system to when the data cell begins to leave the system. Another problem with the conventional implementation is the larger amount of buffer space needed to prevent over and under runs.

Accordingly, what is needed is a smaller data buffer that reduces latency during data transfer. The present invention addresses such a need.

SUMMARY OF THE INVENTION

A data buffer in accordance with the present invention is disclosed. The data buffer comprises an entry section and a signaling circuit coupled to the entry section, the signaling circuit for signaling the data buffer to transfer a portion of a data cell from the entry section prior to the data cell being completely received by the entry section.

Through the use of the data buffer in accordance with the present invention, data transfer systems are improved in two ways. First, by enabling data to be transferred before it is completely stored into the buffer, the latency that is typically required for data cell transfer is reduced. Second, the buffer storage space that is typically required to store a complete data cell is also reduced. This two-fold improvement produces increased data transfer rates while decreasing the amount of required buffer storage space.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an example of a typical data transfer environment.

Figure 2 is a high level flowchart of the method of the present invention.

Figure 3 shows a data buffer in accordance with the present invention.

Figure 4 is a flowchart of the operation of the data buffer in accordance with the preferred embodiment of the present invention.

DETAILED DESCRIPTION

The present invention discloses a data buffer. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

To more particularly describe the method accordance with the present invention, Figure 2 is a simple flowchart of a method in accordance with the present invention. First, data from a data cell is allowed to be written into the data buffer, via step 50. Next, the data cell is read from the data buffer prior to the data cell being completely written into the data buffer, via step 52.

The present invention is presented in the context of a preferred embodiment. The preferred embodiment of the present invention provides an improved asynchronous data buffer. Through the use of the data buffer in accordance with the present invention, data cell transfer latency is reduced. Furthermore, the amount of required buffer storage space is decreased since the buffer storage space that is typically required to store a complete data cell is reduced.

The asynchronous data buffer in accordance with the present invention operates on the premise that programmable data transfer threshold settings can be established in order to allow a data cell to begin being read out of the data buffer prior to the entire data cell being written into the data buffer. Furthermore, the data buffer in accordance with the present invention allows another cell to be written in even if the current cell is not completely read. Preferably, these threshold settings are determined based on mathematical algorithms or empirical data related to the data transfer process. However, one of ordinary skill in the art will readily recognize that a variety of methods could be used to determine the threshold settings while remaining within the spirit and scope of the present invention.

As previously shown, a buffer comprises a write element and a read element. Accordingly, the threshold settings are derived based on the knowledge that at a certain point during the data transfer process, the read element can't possibly get ahead of the write element, even if it is running faster. The reverse is true for the write element. After a certain amount of the data cell has been read out of the data buffer, this amount being less than the full amount, the write element can begin writing a subsequent data cell into the buffer with no danger of data corruption.

It should also be noted that the asynchronous operation of the data buffer in accordance with the present invention is not simply limited to equal but out of phase frequencies. The asynchronous data buffer in accordance with the present invention can operate with two distinctly different frequencies. For example, the write side may run at 10ns, while the read side may run at 8ns. The decoupling of the read and write sides, along with the communication between the two sides via the asynchronous signaling circuitry allows for this type of flexibility when the threshold settings are properly tuned.

In order to facilitate the method in accordance with the present invention, a read-signal is provided to the data buffer once the data cell being transferred has reached the threshold setting (i.e. before the entire data cell is written into the buffer). Once the read-signal is provided, the data buffer begins reading the partially written data cell out of the data buffer. In addition, as the data cell is being read out of the buffer, a write-signal is provided to indicate that a subsequent data cell can begin being written into the data buffer. Although the write-signal is provided prior to the initial data cell being completely read from the data buffer, the threshold settings are established so that data corruption is avoided. Data being read out of the buffer can be corrupted if a subsequent data cell being written into the buffer "catches up" with the data being read out of the buffer and overwrites it.

To better understand the present invention, Figure 3 shows a data buffer in accordance with the present invention. The data buffer comprises a write element (writer) 100, a buffer entry section 150 and a read element (reader) 200. The writer 100 and the reader 200 comprise similar logic structures. The writer 100 and reader each comprise an entry pointer 102, 202 which indicates which data cell is currently being transferred; an item pointer 104, 204 which indicates which specific portion of the data cell is being transferred; and an entry counter 106, 206 which counts how many data cells have been processed (i.e., the write element's entry counter 106 indicates how many data cells have been written but not read and the read element's entry counter 206 indicates how many data cells are left).

The data buffer in accordance with the present invention also includes an asynchronous circuit 152. The asynchronous circuit 152 includes an "add" signaling portion 154 and a "remove" signaling portion 156 and is employed to allow the writer 100 and reader 200 to communicate with each other. Using conventional methodology, a reader is designed to read a

data cell from the buffer entry section only when the data cell has been completely written into the buffer entry section. However, by utilizing the data buffer in accordance with the present invention, data is transferred with a finer granularity.

What is meant by a finer granularity is that the data buffer in accordance with the present invention is programmed to transfer data cells at a byte-access level. What is meant by a byte- access level is that each of a plurality of portions of the data cell are written into the buffer entry section 150 via a byte-access to the buffer entry section 150. For example, 16 byte-accesses to the buffer entry section 150 are required for an entire data cell to be written into the buffer entry section 150. Accordingly, at a predetermined threshold point, i.e. at a point prior to the entire data cell being written into the buffer entry section 150, the reader can't possibly get ahead of the writer. At this predetermined threshold point, for example after the 8th byte-access, the asynchronous circuit 152 provides a signal to the reader 200 to begin reading the data cell.

Although the above outlined description discloses the utilization of a data cell requiring 16 accesses to the buffer entry section wherein the predetermined threshold point is after the 8th access, one of ordinary skill in the art will readily recognize that the number of required access for a data cell and the respective predetermined threshold could vary while remaining within the spirit and scope of the present invention.

By transferring cells at a finer granular level (i.e. via byte-access as opposed to whole cell accesses), the asynchronous data buffer can overcome inefficiencies in the control logic of buffers downstream from it. For example, for cell transfers from chip to chip, there is an inherent latency in starting and stopping cell transfers. By generating thresholds on a byte-access level, the full and empty signals are more timely and can thus over come these

inefficiencies.

This same concept is also utilized with regard to the writer 100. At another predetermined threshold point prior to the entire data cell being read from the buffer entry section 150, the writer 100 can begin writing a subsequent data cell into the buffer entry section 150 with no danger of corrupting the data being read out of the buffer entry section 150.

To better understand the operation of the data buffer in accordance with the present invention, please refer to Figure 4. Figure 4 is a flowchart of the operation of the data buffer in accordance with the preferred embodiment of the present invention. The process begins with a number of data cells needing to be written into the buffer entry section. First, the writer begins to write the first data cell into the buffer entry section by accessing the buffer entry section, via step 300. Next, the writer's item pointer is incremented each time the writer accesses the buffer entry section to write the first data cell, via step 302. Once the item pointer reaches a predetermined threshold, the predetermined threshold being set at a point before the first data cell is completely written into the buffer entry section, the asynchronous signaling circuit signals the reader to increment its entry counter, via step 304. This is done via the "add" signaling portion. Preferably, before data is written into the buffer entry section, the reader's entry counter is zero. Accordingly, zero cells are available to be read. Once, the reader's entry counter is non-zero, this indicates that the buffer entry section is non-empty and the reader can begin reading data from the buffer entry section.

Next, the reader begins reading the first data cell from the buffer entry section by accessing the buffer entry section, via step 306. The reader's item pointer is then incremented each time the reader accesses the buffer entry section, via step 308. Once the reader's item

pointer reaches a predetermined threshold, the asynchronous signaling circuit signals the writer's entry counter to decrement, via step 310. Preferably, this is done via the "remove" signaling portion of the asynchronous circuit. The writer's entry counter is then decremented, thereby reducing by one the number of data cell entries written, but not read, into the buffer entry section, via step 312. The writer can now begin writing a second data cell entry into the buffer entry section once the first data cell is completely written into the buffer entry section. However, when the total buffers available to write have not been read, the system is characterized as full. Consequently, once the "removed" signal comes to the writer, the system is no longer full and the writer can begin writing another data cell into the buffer entry section.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A data buffer, the data buffer comprising:

an entry section; and

a signaling circuit coupled to the entry section for providing a signal to transfer a portion of a data cell from the entry section prior to the data cell being completely received by the entry section.

2. The data buffer of claim 1 wherein the signal is provided once the amount of data received by the entry section reaches a predetermined threshold.

3. The data buffer of claim 2 wherein the entry section comprises a buffer entry section.

4. The data buffer of claim 3 wherein the signaling circuit comprises an asynchronous signaling circuit.

5. The data buffer of claim 4 wherein the buffer entry section comprises a write element and a read element, wherein the write element and the read element each comprise an entry pointer, an item pointer and an entry counter.

6. The data buffer of claim 5 wherein the asynchronous signaling circuit comprises an add signaling portion and a remove signaling portion.

7. The data buffer of claim 6 wherein the asynchronous signaling circuit provides a signal to the write element to begin writing another data cell into the buffer entry section prior to the data cell being completely read from the buffer entry section wherein the signal is provided based on a predetermined threshold.

8. A data buffer for buffering a data cell, the data buffer comprising:

a buffer entry section including a write element and a read element, wherein the write element and the read element each comprise an entry pointer, an item pointer and an entry counter; and

an asynchronous signaling circuit coupled to the buffer entry section, wherein the asynchronous signaling circuit provides a first signal to the read element to transfer data from the buffer entry section prior to a data cell being completely received by the buffer entry section wherein the signal is provided once the amount of data received by the buffer entry section reaches a predetermined threshold.

9. The data buffer of claim 8 wherein the asynchronous signaling circuit comprises an add signaling portion and a remove signaling portion.

10. The data buffer of claim 9 wherein the asynchronous signaling circuit provides a second signal to the write element to begin writing another data cell into the buffer entry section prior to the data cell being completely read from the buffer entry section wherein the second signal is provided once the amount of data received by the buffer entry section reaches

a predetermined threshold.

11. A data buffer for buffering a data cell, the data buffer comprising:

a buffer entry section including a write element and a read element, wherein the write element and the read element each comprise an entry pointer, an entry counter and an item pointer; and

an asynchronous signaling circuit coupled to the buffer entry section, the asynchronous signaling circuit comprising an add signaling portion and a remove signaling portion, wherein the asynchronous signaling circuit provides a first signal to the read element prior to the data cell being completely written into the buffer entry section and a second signal to the write element prior to the data cell being completely read from the buffer entry section, wherein the first signal is provided once the amount of data received by the buffer entry section reaches a predetermined threshold and the second signal is provided once the amount of data read from the buffer entry section reaches a predetermined threshold.

12. A method of transferring data in a data buffer, the method comprising the steps of:

a) allowing a data cell to begin being written into the data buffer; and

b) reading the data cell from the data buffer prior to the data cell being completely written into the data buffer.

13. The method of claim 12 further comprising:

c) allowing another data cell to begin being written into the data buffer

prior to the data cell being completely read out of the data buffer.

14. The method of claim 13 wherein the data cell comprises a plurality of portions and the data buffer comprises:

a buffer entry section including a write element and a read element; and

an asynchronous signaling circuit coupled to the buffer entry section.

15. The method of claim 14 wherein the asynchronous signaling circuit comprises an add signaling portion and a remove signaling portion.

16. The method claim 15 wherein the write element comprises a first entry pointer, a first item pointer, and a first entry counter and the read element comprises a second entry pointer, a second item pointer and a second entry counter.

17. The method of claim 16 wherein step a) further comprises:

a1) allowing the write element to write each of the plurality of data cell portions to the buffer entry section via an access to the buffer entry section;

a2) incrementing the first item pointer each time the buffer entry section is accessed; and

a3) allowing the asynchronous signaling circuit to provide a signal to the read element once the first item pointer reaches a predetermined threshold.

18. The method of claim 17 wherein the signal of step a3) comprises an add signal.

19. The method of claim 18 wherein step a) further comprises:

a4) incrementing the second entry counter.

20. The method of claim 16 wherein step b) further comprises:

b1) allowing the read element to receive a signal from the asynchronous signaling circuit;

b2) allowing the read element to read each of the plurality of data cell portions from the buffer entry section via an access to the buffer entry section;

b3) incrementing the second item pointer each time the buffer entry section is accessed; and

b4) allowing the asynchronous signaling circuit to provide a signal the write element once the second item pointer reaches a predetermined threshold.

21. The method of claim 20 further comprising:

b5) decrementing the first entry counter.

22. The method of claim 21 wherein the signal of step b1) comprises an add signal and the signal of step b4) comprises a remove signal.

ASYNCHRONOUS DATA BUFFER AND A METHOD OF USE THEREOF

ABSTRACT

An improved asynchronous data buffer is disclosed. The data buffer comprises an entry section and a signaling circuit coupled to the entry section, the signaling circuit for signaling the data buffer to transfer a portion of a data cell from the entry section prior to the data cell being completely received by the entry section. Through the use of the data buffer in accordance with the present invention, data transfer systems are improved in two ways. First, by enabling data to be transferred before it is completely stored into the buffer, the latency that is typically required for data cell transfer is reduced. Second, the buffer storage space that is typically required to store a complete data cell is also reduced. This two-fold improvement produces increased data transfer rates while decreasing the amount of required buffer storage space.

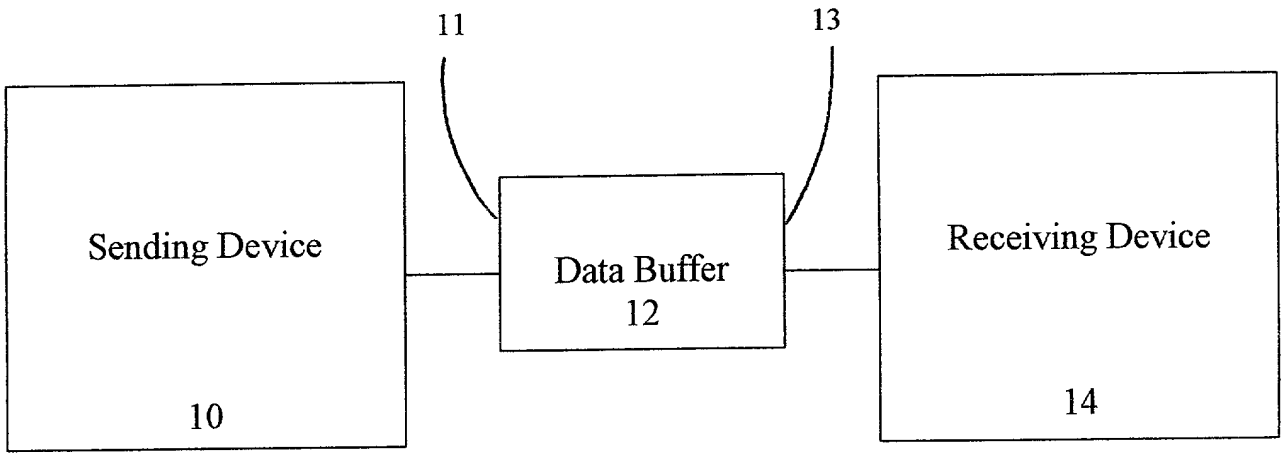

Figure 1
(Prior Art)

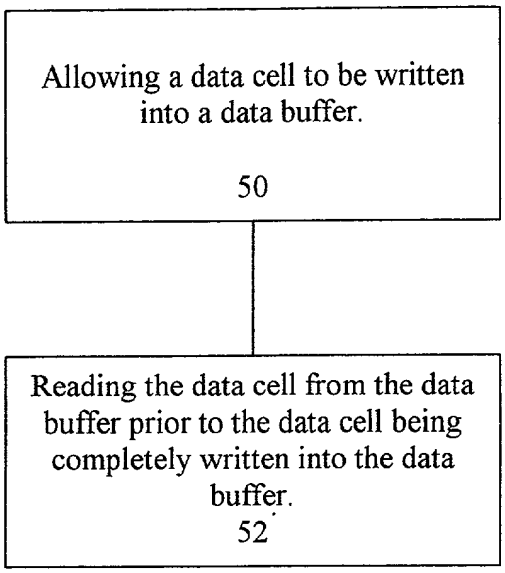
Allowing a data cell to be written into a data buffer.
50
Reading the data cell from the data buffer prior to the data cell being completely written into the data buffer.
52

Figure 2

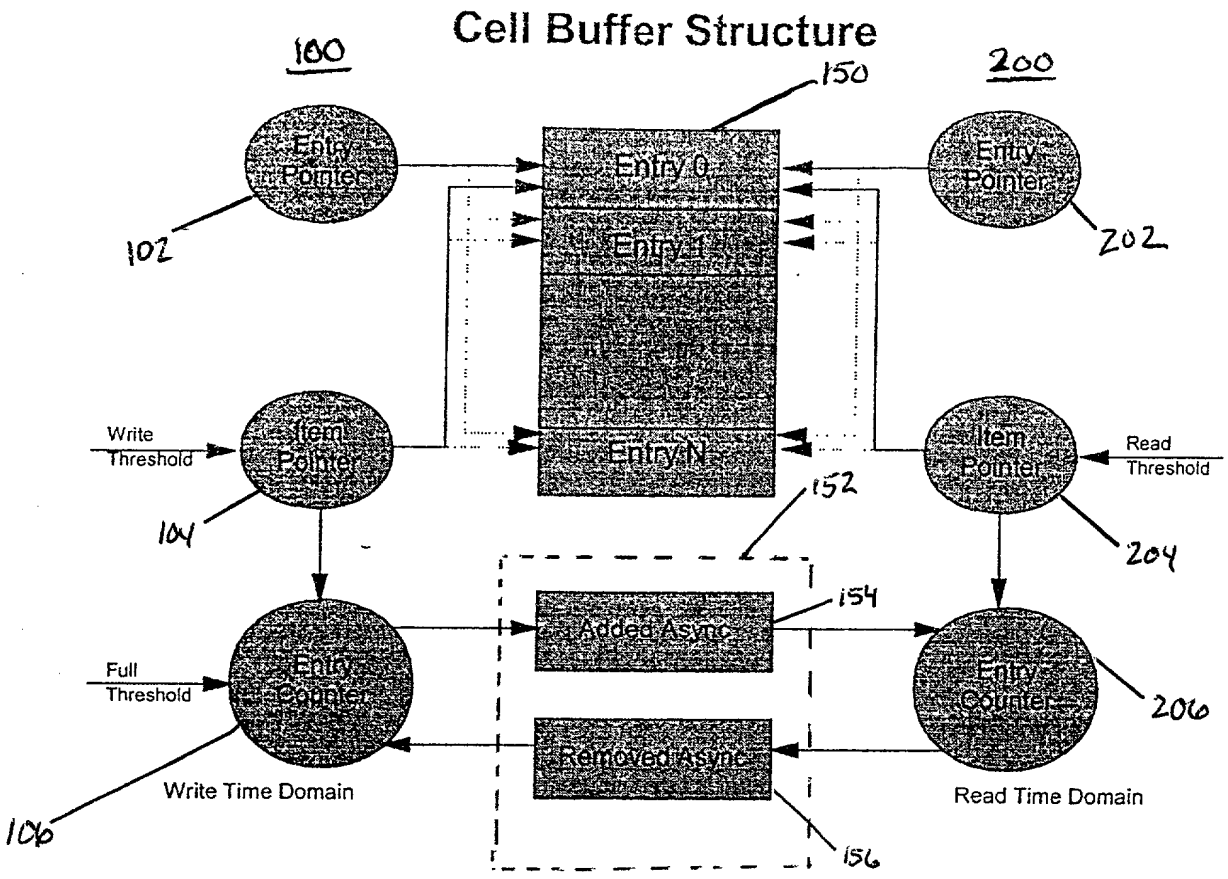
Cell Buffer Structure
100
200
150
Entry Pointer
Entry 0
Entry 1
Entry N
Entry Pointer
102
202
Write Threshold
Item Pointer
Item Pointer
Read Threshold
104
204
152
154
Full Threshold
Entry Counter
Added Async
Entry Counter
206
Removed Async
Write Time Domain
Read Time Domain
106
156

Figure 3

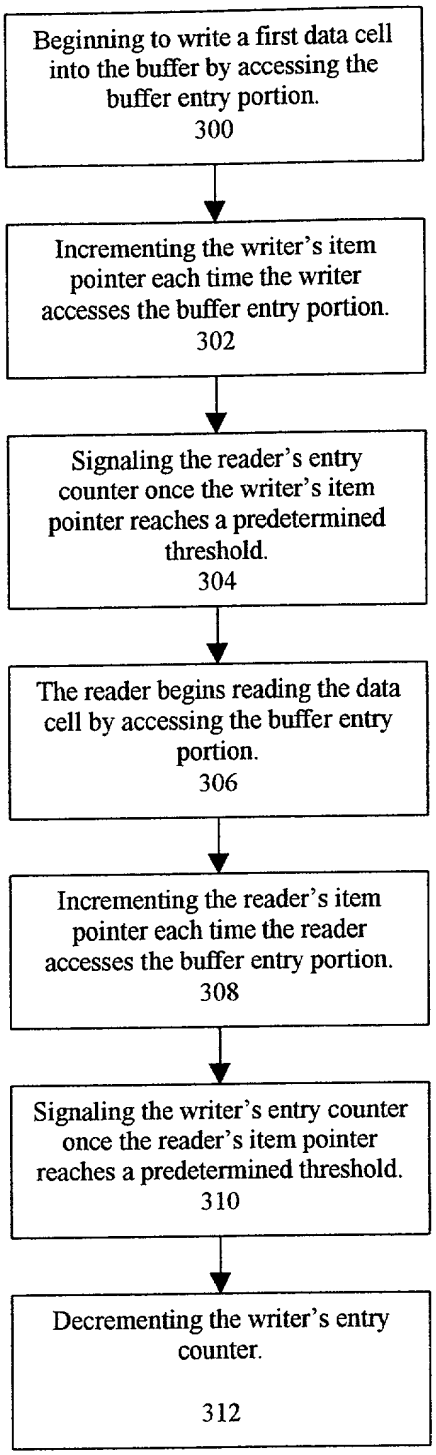
Beginning to write a first data cell into the buffer by accessing the buffer entry portion.
300
Incrementing the writer's item pointer each time the writer accesses the buffer entry portion.
302
Signaling the reader's entry counter once the writer's item pointer reaches a predetermined threshold.
304
The reader begins reading the data cell by accessing the buffer entry portion.
306
Incrementing the reader's item pointer each time the reader accesses the buffer entry portion.
308
Signaling the writer's entry counter once the reader's item pointer reaches a predetermined threshold.
310
Decrementing the writer's entry counter.
312

Figure 4

IBM Docket No. RAL9-99-0137

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ASYNCHRONOUS DATA BUFFER AND A METHOD OF USE THEREOF

the specification of which is identified by the attorney (IBM) Docket Number appearing above.

I hereby state that I have reviewed and understand the contents of the above- identified specification, including the claims.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

Number	Country	Day/Month/Year	Priority Claimed

I hereby claim the benefit (a) under Title 35, United States Code, §119(e) of any U.S. application listed below and identified as a provisional application or (b) under Title 35, United States Code, §120 of any U.S. application listed below and not identified as a provisional application, and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior U.S. application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information material to the patentability of this application as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application

Prior U.S. Applications

Serial No.	Filing Date	Status

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Daniel E. McConnell, Reg. No. 20,360; Kenneth A. Seaman, Reg. No. 28,113; Joscelyn G. Cockburn, Reg. No. 27,069; Gerald R. Woods, Reg. No. 24,144; John D. Flynn, Reg. No. 35,137; Horace St. Julian, Reg. No. 30,329; Joseph C. Redmond, Jr., Reg. No. 18,753; John E. Hoel, Reg. No. 26,279; Christopher A. Hughes, Reg. No. 26,914; and Edward A. Pennington, Reg. No. 32,588.

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